Notice of Allowability	Application No.	Applicant(s)	
	09/815,873	ROSKOWSKI ET AL.	
	Examiner	Art Unit	
	Tammara R. Peyton	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 7/21/05 and Supplemental Oath filed 1/13/06 and Petition granted 3/24/06*.

2. ☒ The allowed claim(s) is/are *1-30*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Drawings

Applicant amended Fig. 3 of the drawings on 08/29/02 and Examiner approves the change to Fig. 3. New corrected drawings (including the change to Fig. 3) in compliance with 37 CFR 1.121(d) are required in this application because the application is in condition for allowance.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. The application has been amended as follows:

3. The following changes to the claims 1, 3, 4, 5, 6, 8, and 14 have been approved by Examiner and agreed upon by applicant's attorney Mr. Amir Raubvogel, Reg. No. 37,070 on March 28, 2006.

Claim 1

A computer system comprising a first component operated in response to timing of a first clock, means for storing information, means for transferring information from the first component to the means for storing information always utilizing the first clock without synchronization to another clock, a second component operated in response to timing of a second clock, the timing of the first clock being independent of the timing of the second clock, means for utilizing the second clock to transfer information without synchronization with the first clock from the means for storing information without transferring other information into said means for storing information whereby the information may be immediately utilized by the second component without need for storage by the second component, said means for utilizing the second clock to transfer information without synchronization with the first clock from said means for storing information comprising means for transferring the information in said means for storing information to the second component under control of the second clock, said means for transferring the information in said means for storing information to the second component under control of the second clock includes means for switching the second clock to the terminals used by the first clock, said means for switching the second clock to the terminals used by the first clock, said [multiplexor] multiplexer receiving a signal from the second component for furnishing a second clock signal from said second clock to said means for storing information to transfer information to said second component.

Claim 3

A computer system as claimed in claim 1 in which the means for switching the second clock to the terminals used by the first clock includes means for signaling the [multiplexor] multiplexer that the second component is ready to accept the information in the means for storing information.

Claim 4

A computer system comprising a plurality of components operated in response to timing of different clocks, means for storing information, means for utilizing the clock of any one of the components to transfer information without synchronization of timing of different clocks between one of the components and the means for storing information, means for signaling any of the components that information stored in the means for storing is to be transferred to that one of the components as a destination component, means for utilizing the clock of the destination component to transfer information from the means for storing information without synchronization of timing of different clocks in a condition in which the information is synchronized for use by the destination component wherein the means for utilizing the clock of any one of the components always utilizes the clock of the component transferring information into said means for storing information, and wherein the timing of the clock of the component from which the information was transferred is independent of the timing of he clock of the destination

component, said means for utilizing the clock of the destination component to transfer information from the means for storing information in a condition in which it is synchronized for use by the destination component includes a [multiplexor] multiplexer for transferring signals from the destination component to the means for storing information, said [multiplexor] multiplexer coupled to the component transferring information into the means for storing information and the destination component, said [multiplexor] multiplexer receiving a signal from said the destination component for furnishing a clock signal from the clock of the destination component to the means for storing information to transfer information to the destination component.

Claim 5

A computer system as claimed in claim 4 in which the means for signaling a second destination component that the information stored in the means for storing information is to be transferred to the second destination component comprises means for synchronizing a signal from the means for [signalling] signaling with the clock of the second destination component.

Claim 6

A computer system as claimed in claim 4 in which the [multiplexor] multiplexer

comprises an AND gate, and means for transferring gated clock signals from each of the components as inputs to the AND gate.

Claim 8

A computer system comprising:

a first component;

a first clock coupled to said first component, said first component operated in response to timing of said first clock;

a buffer coupled to said first component, said first component always using said first clock to transfer data from said first component to said buffer without synchronizing said transfer of said data to another clock;

a second component coupled to said buffer;

a second clock coupled to said second component, the timing of said first clock being independent of the timing of said second clock, said second component reading said data from said buffer using said second clock without synchronizing said reading to another clock and without transferring other data into said buffer;

a [multiplexor] multiplexer coupled to said first component and said second component, said [multiplexor] multiplexer receiving a signal from the second component for furnishing a second clock signal from said second clock to said buffer to transfer data to said second component.

Claim 14

A method for transferring data between a plurality of components in a computer system including a first and a second component, said method comprising:

operating said first component using a first clock having a first timing;

operating said second component using a second clock having a second timing independent of said first timing;

transferring an entire packet of data having a plurality of words from said first component to a buffer always using said first clock without synchronizing any of said plurality of words to another clock;

once said entire packet of data is transferred from said first component to said buffer, signaling said second component that said entire packet of data is ready to be transferred to said second component;

transferring said entire packet of data to said second component using said second clock without transferring other data into said buffer;

furnishing a clock signal to said buffer from a [multiplexor] multiplexer, said [multiplexor] multiplexer coupled to said first component and said second component, said [multiplexor] multiplexer receiving a signal from the second component for furnishing a second clock signal from said second clock to said buffer to transfer data to said second component.

EXAMINER'S REASON FOR ALLOWANCE

4. The following is an examiner's statement of reasons for allowance: the prior art of record does not teach or suggest individually or in combination the limitation of a computer system comprising a first component operated in response to timing of a first clock, means for storing information, means for transferring information from the first component to the means for storing information always utilizing the first clock without synchronization to another clock, a second component operated in response to timing of a second clock, the timing of the first clock being independent of the timing of the second clock, means for utilizing the second clock to transfer information without synchronization with the first clock from the means for storing information without transferring other information into said means for storing information whereby the information may be immediately utilized by the second component without need for storage by the second component, said means for utilizing the second clock to transfer information without synchronization with the first clock from said means for storing information comprising means for transferring the information in said means for storing information to the second component under control of the second clock, said means for transferring the information in said means for storing information to the second component under control of the second clock includes means for switching the second clock to the terminals used by the first clock, said means for switching the second clock to the terminals used by the first clock, said multiplexer receiving a signal from the

second component for furnishing a second clock signal from said second clock to said means for storing information to transfer information to said second component.

2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammara Peyton whose telephone number is (571) 272-4157. The examiner can normally be reached between 6:30 - 4:00 from Monday to Thursday, (I am off every first Friday), and 6:30-3:00 every second Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Popovici Dov can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Mailed responses to this action should be sent to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231.

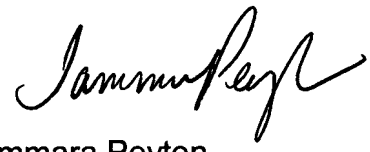
Faxes for Official/formal (After Final) communications or for informal or draft communications (please label "PROPOSED" or "DRAFT") sent to:

(571) 273-8300

Hand-delivered responses should be brought to:

USTPO, Randolph Building, Customer Service Window
401 Dulany Street
Alexandria, VA 22314.

TAMMARA PEYTON
PRIMARY EXAMINER



Tammara Peyton
March 28, 2006